AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor element formed in a surface of a wafer including a transistor portion;

an external connection terminal connected electrically to the semiconductor element which has at least one electrode formed in the surface of the wafer; and

an electrically insulating layer provided between the semiconductor element and the external connection terminal,

wherein the electrically insulating layer has an edge on the surface of the wafer to expose the at least one electrode of the semiconductor element therefrom,

wherein the transistor portion is covered with a portion of the electrically insulating layer, and

wherein the said portion of the electrically insulating layer has a thickness in a range of from 35 to 150 micrometers.

2. (Cancelled without prejudice or disclaimer.)

3. (Currently Amended) A semiconductor device ~~according to claim 2,~~ comprising:

a semiconductor element formed in a surface of the semiconductor device including a transistor portion and at least one electrode;

an external connection terminal connected electrically to the semiconductor element through at least one electrode; and

an electrically insulating layer provided between the semiconductor element and the external connection terminal,

wherein the electrically insulating layer has an edge between the transistor portion and the at least one electrode on the surface of the semiconductor device and exposes the at least one electrode of the semiconductor element therefrom,

wherein the transistor portion is placed in an outer circumferential portion of the [semiconductor element] surface of the semiconductor device with respect to the at least one electrode, and

wherein the transistor portion is covered with a portion of the electrically insulating layer having a thickness in a range from 35 to 150 micrometers.

4. (Original) A semiconductor device according to claim 1,

wherein the semiconductor element includes a memory cell, and

wherein the electrically insulating layer is provided to cover at least the memory cell.

5. (Original) A semiconductor device according to claim 1,

wherein the external connection terminal is a solder bump.

6. (Original) A semiconductor device according to claim 5,

wherein the electrically insulating layer is formed of polyimide material.

7. (Original) A semiconductor device according to claim 1,

wherein the electrically insulating layer is formed of polyimide material.

8. (Currently Amended) A semiconductor device according to claim 1,

~~wherein the semiconductor element includes a transistor portion, and~~

wherein ~~a~~ the thickness of a the portion of the electrically insulating layer covering the transistor portion of the semiconductor element is greater than a thickness of another portion of the electrically insulating layer covering a different portion of the semiconductor element from the transistor portion.

9. (Currently Amended) A semiconductor device according to claim 8,

wherein the external connection terminal ~~is~~ has a solder bump provided thereon.

10. (Original) A semiconductor device according to claim 9,

wherein the electrically insulating layer is formed of polyimide material.

11. (Currently Amended) A semiconductor device ~~according to claim 8,~~ comprising:

a semiconductor element having a transistor portion and at least one electrode spaced from a transistor portion;

an electrically insulating layer covering at least the transistor portion and having an edge between the transistor portion and the at least one electrode; and

an external connection terminal formed on the electrically insulating layer and connected electrically to the at least one electrode of the semiconductor element,

wherein the electrically insulating layer includes a first portion having a thickness in a range of from 35 to 150 micrometers with which the transistor portion is covered and a second portion at the edge thereof, and

wherein the transistor portion is placed in an outer circumferential portion of the semiconductor ~~element~~ device with reference to the at least one electrode.

12. (Currently Amended) A semiconductor device according to claim 8,

wherein the external connection terminal is a solder bump, the solder bump has a thickness determined by its location relative to the ~~different~~ thicknesses of a part of the electrically insulating layer on which the external connection terminal is formed.

13. (Original) A semiconductor device according to claim 12,

wherein the electrically insulating layer is formed of polyimide material.

14. (Currently Amended) A semiconductor device comprising:

a semiconductor element ~~with~~ having a transistor portion and

at least one electrode~~,~~ spaced from a transistor portion;

an electrically insulating layer covering at least the transistor portion but not the at least one electrode; and

an external connection terminal formed on the electrically insulating layer and connected electrically to ~~an~~ the at least one electrode of the semiconductor element,

~~wherein the semiconductor element includes a transistor portion,~~

wherein ~~an~~ the electrically insulating layer ~~is provided between the semiconductor device and the external connection terminal to cover at least~~ includes a first portion with which the transistor portion is covered and a second portion at an edge thereof close to the at least one electrode, and

wherein the first portion of the electrically insulating layer has a thickness in a range of from 35 to 150 micrometers.

15. (Currently Amended) A semiconductor device according to claim 14,

wherein the external connection terminal is a solder bump, and

wherein the electrically insulating layer intercepts an α-ray generated from the solder bump reaching the transistor portion.

16. (Original) A semiconductor device according to claim 15,

wherein the electrically insulating layer is formed of polyimide material.

17. (Original) A semiconductor device according to claim 14,

wherein the electrically insulating layer is formed of polyimide material.

18. (Currently Amended) A semiconductor device for flip-chip mounting on a wiring board, comprising:

a semiconductor element ~~with~~ including a transistor portion and at least one electrode~~,~~ spaced from the transistor portion, both arranged in a surface of the semiconductor device;

an external connection terminal connected electrically to ~~an~~ the at least one electrode of the semiconductor element,

~~wherein the semiconductor element includes a transistor portion,~~

wherein an electrically insulating layer is provided between the semiconductor device and the external connection terminal and includes a portion to cover at least the transistor portion ~~with a portion thereof~~, ~~and~~

wherein the electrically insulating layer has an edge thereof on the surface of the semiconductor device between the transistor portion and the at least one electrode of the semiconductor element to expose the at least one electrode therefrom, and

wherein the said portion of the electrically insulating layer is spaced from the edge thereof and has a thickness in a range of from 35 to 150 micrometers.

19. (Currently Amended) A semiconductor device according to claim 18,

wherein the external connection terminal is a solder bump, and

wherein the electrically insulating layer intercepts an α-ray generated from the solder bump reaching the transistor portion.

20. (Original) A semiconductor device according to claim 18, wherein the electrically insulating layer is formed of polyimide material.

21. (New) A semiconductor device according to claim 1, wherein the electrically insulating layer has an inclined portion thereof at the edge thereof.

22. (New) A semiconductor device according to claim 21, wherein the transistor portion of the semiconductor element is positioned so as to be covered with the portion of electrically insulating layer not containing the inclined portion thereof.

23. (New) A semiconductor device according to claim 21, wherein the external connection terminal and the at least one electrode are electrically connected to each other by a wiring formed on the electrically insulating layer and extended beyond the edge of the electrically insulating layer to the at least one electrode.

24. (New) A semiconductor device according to claim3, wherein the electrically insulating layer has an inclined portion thereof at the edge thereof, and the portion thereof covering the transistor portion is

spaced from the edge thereof by the inclined portion thereof.

25. (New) A semiconductor device according to claim 24,

wherein the inclined portion of the electrically insulating layer is inclined at a gradient of from 5 to 30% with respect to the surface of the semiconductor device.

26. (New) A semiconductor device according to claim 8,

wherein the said another portion of the electrically insulating layer covering the different portion of the semiconductor element from the transistor portion is located between the portion thereof covering the transistor portion and the edge thereof.

27. (New) A semiconductor device according to claim 11,

wherein the second portion of the electrically insulating layer is inclined, and the first portion thereof is spaced from the edge thereof by the second portion thereof.

28. (New) A semiconductor device according to claim 14,

wherein the second portion of the electrically insulating layer is inclined at an average gradient of from 5 to 30%.

29. (New) A semiconductor device according to claim 14,

wherein the second portion of the electrically insulating layer is inclined,

and the external connection terminal is electrically connected to at least one electrode of the semiconductor element through a wiring formed on the second portion thereof and extended beyond the edge thereof to the at least one electrode not covered by the electrically insulating layer.

30. (New) semiconductor device according to claim 18,

wherein the thickness of the portion of the electrically insulating layer covering at least the transistor portion is 1/20 to 1/5 as large as a thickness of the semiconductor device.

31. (New) A semiconductor device according to claim 18,

wherein the semiconductor device is connected to a circuit substrate with a solder bump provided on the external connection terminal.